IN THE SPECIFICATION:

Please replace the paragraph beginning on page 2, line 7, through page 2 line 20, with the following paragraph.

Turning to **Figure 1**, a block diagram of a known semidigital DLL-based CDR using a phase rotator is shown. This prior art CDR includes DLL or PLL circuit **100**, phase rotator **102**, phase detector/sampler (PD/S) **104**, and digital finite state machine (FSM) **106**. DLL or PLL circuit **100** receives a clock reference signal, CLK_{ref}. The output of DLL or PLL circuit **100** is input into phase rotator **102**. In turn, phase rotator **102** generates an output clock signal, CLK_{out} at a frequency commensurate with that of CLK_{ref} and with a phase shift controlled by the action of the phase rotator. Phase detector/sampler **104** receives a digital data stream, DAT_{in}, and a clock signal, CLK_{out}, used to generate information about the phase relationship between CLK_{out} and DAT_{in} and to sample DAT_{in}. Phase detector/sampler **104** also generates an output data stream, DAT_{out}. Phase detector/sampler **104** generates up (UP) or down (DN) signals in a digital data stream, which is received by digital finite state machine (FSM) **106**. In turn, digital finite state machine **106** processes this information to produce appropriate control signals which are sent to phase rotator **102**.

Please also replace the paragraph beginning on page 19, line 6 through line 12 with the following paragraph.

A low-power full-rate semidigital DLL architecture using an analog-based FSM (AFSM). The AFSM is a mixed-mode FSM in which analog integration is substituted for digital filtering, thus enabling a lower power implementation of the clock and data recovery function. An integrated voltage is converted to a digital code by an analog-to-digital converter (ADC), and the digital code is used either directly or after (low frequency) digital signal processing to control a [[a]] controllable delay element, such as, a phase rotator, for data edge tracking.